PATENT
Our Docket No.: 44176.00033

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Date: March 14, 2002 By: Margaret A. Turiano 4/16/02
Margaret A. Turiano

In re Application of:

Ejaz Ul Haq

Serial No. 09/851,622 Examiner: Le, D.

Filing Date: May 8, 2001 Art Unit: 2816

Title: High Speed Source Synchronous Signaling For Interfacing VLSI CMOS Circuits To Transmission Lines

Honorable Commissioner of Patents
Washington, D.C. 20231

AMENDMENT AND RESPONSE

Sir:

In response to the Office Action dated October 11, 2001, please amend the application as follows. A petition for a three (3) month extension of time is attached.

In The Specification:

The paragraph beginning at **page 10, line 3** has been amended to read as follows:

As shown in FIG. 3A, the SSVTR and /SSVTR signals toggle every time valid signals are driven by the master 205. It will be appreciated that slave 210 may include multiple receivers (405, FIG. 4), wherein each receiver 405 includes two comparators, one for comparing the signal against SSVTR and the other for comparing the signal against /SSVTR. A present signal binary value determines which comparator is coupled to the output terminal 420, optionally by using exclusive-OR logic with SSVTR and